

A Review on VDMOS as a Power MOSFET

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ABSTRACT: Today's electronics scenario finds itself with advancement in the field of fore most important component MOSFET. Though one step ahead of MOSFET, power MOSFETs find prime and superior choice for discrete components in circuits as well as today's integrated circuits. Moreover the revolutionary usage of power mosfet for significant power handling capacity lead to the discovery of a whole new genre of power Mosfet such as VDMOS. The progressive demand for high power radio frequency applications in wireless market and superior switching speed makes VDMOS a worthy choice. This paper actuates the working model of VDMOS with its characteristics and working parameters such as breakdown voltage, on-resistance etc.

Keywords - Commutation, Power Mosfet, Transconductance, V-groove MOSFET, Vertical diffused MOSFET

I. INTRODUCTION

VDMOS has highly accomplished features of large input impedance, high switching speed and well heat stability. Its wide range of features have been applied to motor drive, switch power supply, automotive electronics and energy saving lamp and so on.

The development of power MOSFETS began in 1970s VMOS (vertical *MOSFET*), after a decade DDMOS (double diffused *MOSFET*) technology was introduced. The VDMOS (vertically diffused *MOSFET* and LDMOS (laterally diffused *MOSFET*) were derived from the DDMOS technology. Thus the first generation of VDMOS was launched. Currently, the development of VDMOS in our country is still in its prime and the research is still in its maturing stage.

A high blocking voltage in the off-state and a high current capacity in the on-state – two characteristics associated with power devices – usually exceed the limitations of modern conventional transistors to perform as a high-power switch. The on-resistance of a VDMOS is one of its most important parameters because it limits the current which can be conducted by the device before it is damaged by the heat generated in the transistor. Therefore the on-resistance should be as low as possible. Another important parameter is the maximum blocking voltage. This is the maximum voltage applied between the source and drain contacts with zero gate-source voltage which does not lead to breakdown.

All power semiconductor devices work on the objective of obtaining high breakdown voltage (BV) (up to 100 volts) in OFF state while keeping the area specific on-resistance R_{on} as low as possible. The capability of VDMOS to produce high breakdown voltage of about 100V makes it a commonly used power device, for example, in automotive electronics. While there are more growth areas as there remains a drawback of VDMOS i.e. the high value of the on-resistance when meeting the breakdown voltage requirement.

Device characteristics of a power VDMOS transistor are more of like those of conventional MOS transistors. The active region of a power VDMOS transistor consists of four distinct regions between the source region (formed by n+ diffused region) and the substrate region (n+ drain region). This can be seen in Fig.1. In this figure, region A is the surface layer of the body region. The channel will form at this region at a given gate bias. Region B is the surface layer of the body region between the source diffusions. Region C is the regions between body regions. Region D is the drain drift region in the epilayer. Region A controls the flow of current in the device, whereas any blocking voltages are developed across the region D.

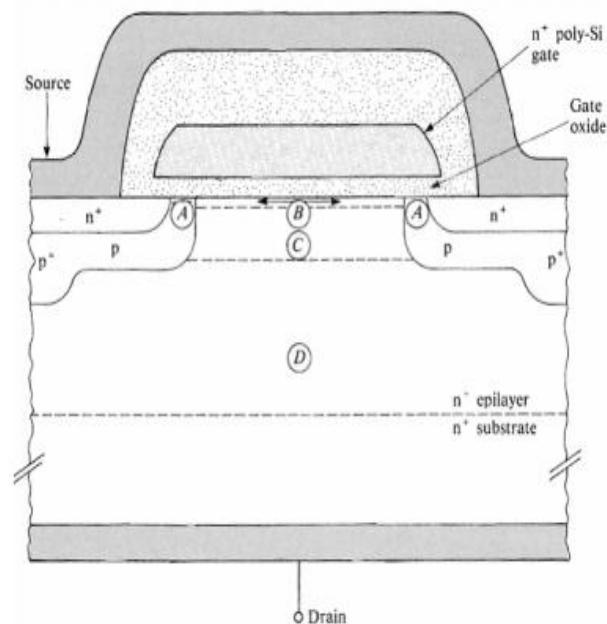


Fig.1: Schematic View of VDMOS

II. CONVENTIONAL MOS VS VDMOS

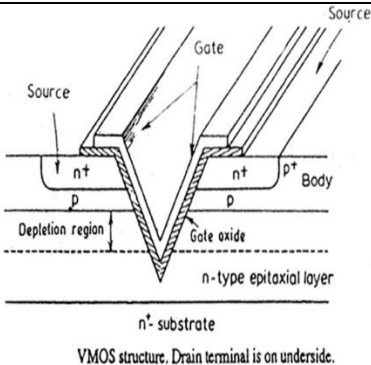
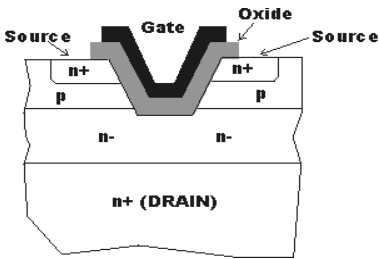
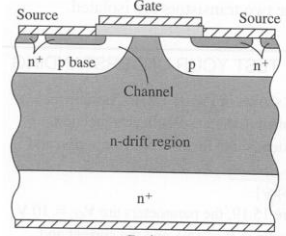
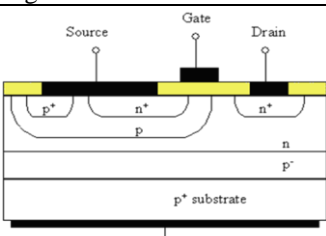
While connecting together various MOSFETS in parallel may enable us to switch high currents or high voltage loads, doing so becomes expensive and impractical in both components and circuit board space. To overcome this problem Power Field Effect Transistors or Power FET's like VDMOS were developed.

The major disadvantages of lateral MOSFET are high resistance channels. In normal operation, the source is electrically connected to the substrate. With no gate bias, the depletion region extends out from the N+ drain in a pseudo hemispherical shape. The channel length L cannot be made shorter than the minimum depletion width required supporting the rated voltage of the device. Channel resistance may be decreased by creating wider channels but this is costly since it uses up valuable silicon real estate. It also slows down the switching speed of the device by increasing its gate capacitance. . Device Ruggedness The ruggedness of Power MOSFET can be described by the following three major characteristics. 1. Avalanche Energy 2. Commutating dv/dt Capability 3. Forward-Biased Safe Operating Area (FBSOA) Capability.

The cross section of a VDMOS shows the "verticality" of the device: it can be seen that the source electrode is placed over the drain, resulting in a current mainly vertical when the transistor is in the on-state. The "diffusion" in VDMOS refers to the manufacturing process: the P wells are obtained by a diffusion process (actually a double diffusion process to get the P and N+ regions, hence the name double diffused). Power MOSFETs have a different structure from the lateral MOSFET: as with most power devices, their structure is vertical and not planar. In a planar structure, the current and breakdown voltage ratings are both functions of the channel dimensions (respectively width and length of the channel), resulting in inefficient use of the "silicon estate". With a vertical structure (VDMOS), the voltage rating of the transistor is a function of the doping and thickness of the N epitaxial layer (see cross section), while the current rating is a function of the channel width. This makes possible for the transistor to sustain both high blocking voltage and high current within a compact piece of silicon.

The Table I shows the main difference between LDMOS (laterally diffused MOS) transistor and a VMOS, DDMOS, UMOS transistor is that it has a lateral current-flow pattern. Thus, LDMOS transistor offers higher speed in comparison to all power MOSFET configurations.

Table 1. Various Configurations of Power MOSFET

S.No.	Configuration	Structure	Description	Breakdown voltage	$R_{DS\ ON}$
1	VMOS (Vertical MOSFET)	 <p>Fig. 2 Vmos structure</p>	VMOS is used for describing the V-groove vertically cut into the substrate material.	The breakdown voltage will be almost greater than or equal to 50 Volts.	3Ω
2	UMOS	 <p>Fig. 3 Umos structure</p>	The bottom of the V in VMOS is flattened out to give it a U shape - hence the name UMOS.	Exhibit breakdown voltages ranging from 35 to 45V with a current handling capability of 1A.	0.21 mΩcm ²
3	DDMOS (Double diffused MOSFET)	 <p>Fig.4 DDMOS structure</p>	The DDMOS device uses a double diffusion process.	Breakdown voltage is less than 50V.	0.245 mΩcm ²
4	LDMOS (Laterally diffused MOSFET)	 <p>Fig.5 LDMOS structure</p>	The Laterally Diffused MOSFET (LDMOS) is an asymmetric power MOSFET designed for low on-resistance and high blocking voltage.	Breakdown voltage of Ldmos can be as low as 20v and as high as 80v.	2.78 mΩ

III. DESIGN PARAMETERS OF VDMOS

Threshold Voltage

A threshold voltage (V_T) of a MOS transistor is defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistors. When enough voltage is applied at the gate (V_T), enough electrons accumulate under the gate to cause an

inversion layer in Region A. This forms a conductive channel across Region A. Electrons now flow in either direction through the channel. As electrons move from the source towards the drain, the forward positive drain current flows into the source. The process of channel formation (depletion and inversion). A typical power MOSFET V_T are 2 to 4 V for high voltage devices with thicker gate oxides and 1 to 2 V for lower voltage devices with thinner gate oxides.

Output characteristic curve for VDMOS

The typical set of output characteristics (also known as family of curves) for a power VDMOS transistor is shown in Fig.6. For each curve, gate to source voltage (V_{GS}) is constant.

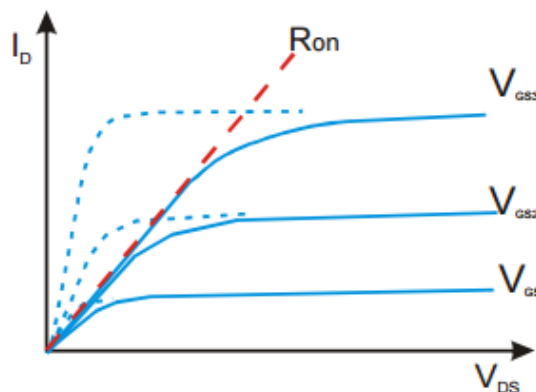


Fig.2: Output IV Curves of a VDMOS [9]

The drain current can be calculated using Equations (1) or (2) depending on the region of operation.

$$I_D = k[(V_{GS} - V_T)V_{Ch} - \frac{1}{2}V_{Ch}^2] \quad (1)$$

$$I_D = \frac{1}{2}K(V_{GS} - V_T)^2 \quad (2)$$

Where k is known as the device transconductance parameter and V_{Ch} is the voltage drop along the channel inversion layer which excludes the influence of series resistance.

$$K = \mu_n \left(\frac{W}{l}\right) C_{ox} \quad (3)$$

Where μ_n is the electron channel mobility, w is the channel width, l is the channel length, and C_{ox} is the capacitance per unit area of the gate oxide.

As compared with VDMOS, for conventional MOSFET we have

$$I_{D(LINEAR)} = \mu C_{ox} \frac{w}{l} (2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2)/2 \quad (4)$$

$$I_{D(SAT)} = \mu C_{ox} \frac{w}{l} (V_{GS} - V_{TH})^2/2 \quad (5)$$

From above equations (4) and (5), we can say that in VDMOS there is the channel voltage between the drain and source V_{Ch} , whereas in the conventional MOSFET we have the drain to source voltage (V_{DS}).

On Resistance ($R_{DS, ON}$): The on-resistance of a VDMOS is one of its most important parameters because it limits the current which can be conducted by the device before it is damaged by the heat generated in the transistor. Therefore the on-resistance should be as low as possible.

The total on-state resistance of a power VDMOS transistor ($R_{DS, ON}$) is expressed as the sum of several different terms: the resistance of the inverted channel (R_{CH}), the spreading resistance of the accumulation region formed in the surface of the epilayer (R_A), the resistance of the bulk semiconductor – the drain region (R_{DO}), and the resistance of the substrate (R_{SUB}) as shown in Equation (6),

$$R_{DS(on)} = R_{CH} + R_A + R_{DO} + R_{Sub} \quad (6)$$

R_{DO} is separated further into R_J and R_D , where R_J is the spreading resistance within the space between the p-body regions (also referred to as the JFET region), and R_D is the resistance occurring under the p-body to the

top of the substrate. R_{n+} , which can be added to the total on-state resistance, is the resistance of the source region (n+) and is negligible compare to other components that form $R_{DS(on)}$.

$R_{DS(on)}$ increases with temperature due to the decreasing carrier mobility. This is an important characteristic for device paralleling.

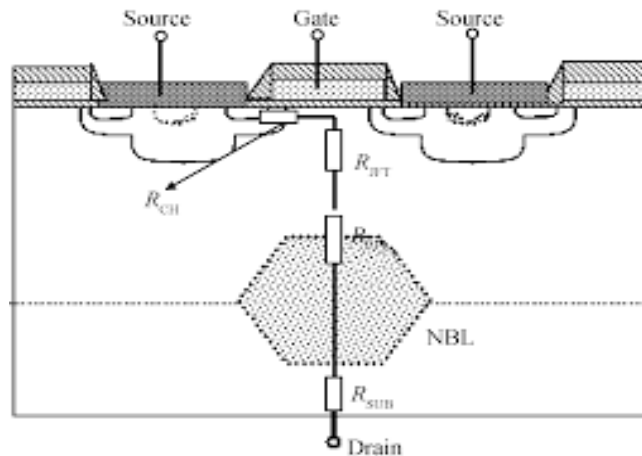


Fig.3 VDMOS on Resistance

Decreasing $R_{DS(on)}$: Low $R_{DS(on)}$ values are needed to maintain a low resistive loss associated with the MOS transistors. Having a lower value of $R_{DS(on)}$ both minimizes the static on-state power loss of devices and maximizes the current rating of the devices. Minimizing $R_{DS(on)}$ provides device with superior power-switching performance since the voltage drop from drain to source is also minimized for a given value of drain-to-source current.

Increasing $R_{DS(on)}$: Since the mobility of holes and electrons decreases as temperature increases, $R_{DS(on)}$ is dependent on the temperature.

Breakdown Voltage: Breakdown voltage (BV_{DSS}) is the maximum voltage between drain to source that a MOS transistor can handle without causing avalanche breakdown of the p n junction formed at the body-drain region in the off-state. There are five driving factors controlling breakdown: avalanche, reach-through, punch-through, Zener, and dielectric breakdown.

The value of $R_{DS(on)}$ normally increases with increasing breakdown voltage. It is desired to have low $R_{DS(on)}$ and high Breakdown voltage values, the tradeoff makes it a difficult task to specify the optimum doping and thickness of the n- epilayer.

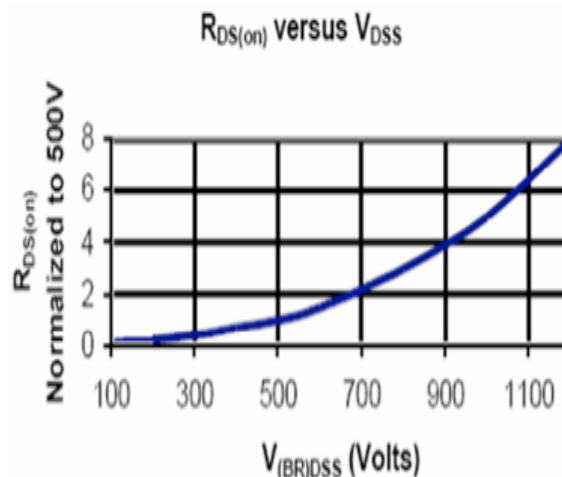


Fig. 4 on Resistance V\ S Breakdown Voltage

$$\text{Also } R_{DS(on)} \propto BV_{DSS} \quad (7)$$

IV. CHARACTERISTIC CURVE OF VDMOS

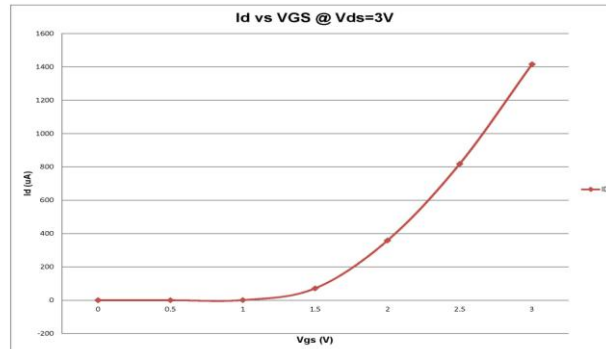


Fig.5 Drain Current $V \setminus S$ Gate To Source Voltage.

The characteristic curve of VDMOS as represented above lets us know the different regions of working of VDMOS with the drain voltage increasing with the gate voltage until it becomes saturated.

V. CONCLUSION

The main advantages of VDMOS are high commutation speed and good efficiency at low voltages. The only limitation of this type of MOSFET is the poor on-state performance. The wide range of applications of VDMOS deals with RF applications, automotive applications, power supply (switching), DC\DC converters, VRM (Voltage regulator module), motor drive applications, IPMCM (intelligent power multichip module).

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